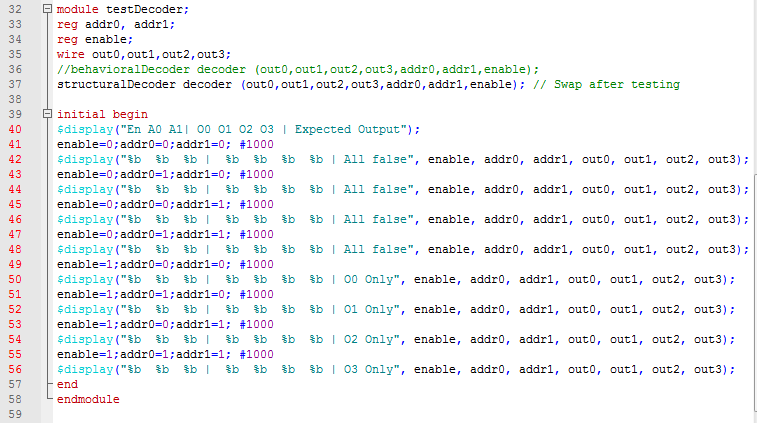
Computer Architecture HW2.

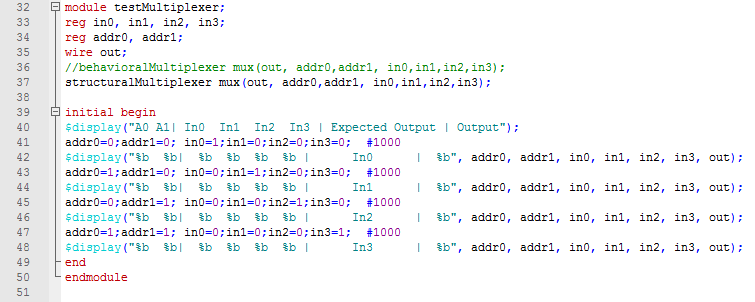
***(Jake) YoonTae Jung***

1. Test-benches
   1. Decoder testbench



Test bench of decoder was offered by the professor and it shows the truth table by changing the enable and inputs.

* 1. Multiplexer test-bench



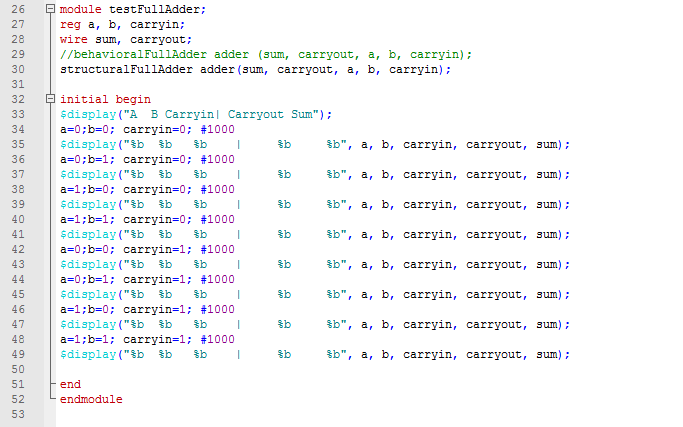
The 4bit-Mux selects one input among 4 inputs by using selectors. There are 4 cases of 2 bit selectors and each of the case represents one output.

When (addr0, addr1)=(0,0) the output becomes In0

(addr0,addr1)=(1,0) 🡪 output: In1 , (addr0, addr1)=(0,1) 🡪output: In2, (addr0, addr1)=(1,1) 🡪 In3

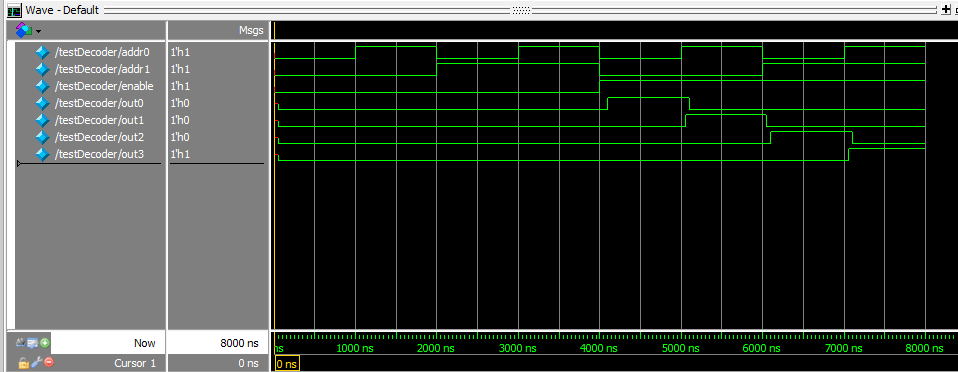
To show this I mad expected output to be HIGH and the others to LOW. Therefore only one input is HIGH and the others are LOW in the truth table.

* 1. FullAdder test-bench



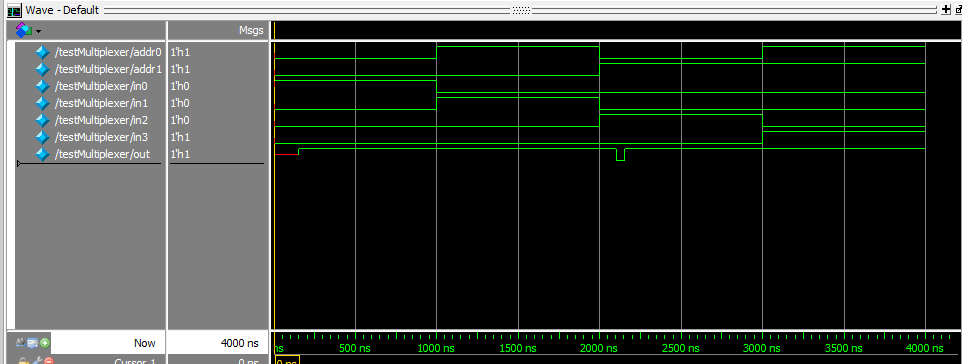
The structuralFullAdder get inputs a, b, carryin and outputs sum and carryout. To show the truth table I designed the all cases of 8 and showed all inputs and outputs from the FullAdder.

1. Waveform(propagation delay)
2. Decoder waveform



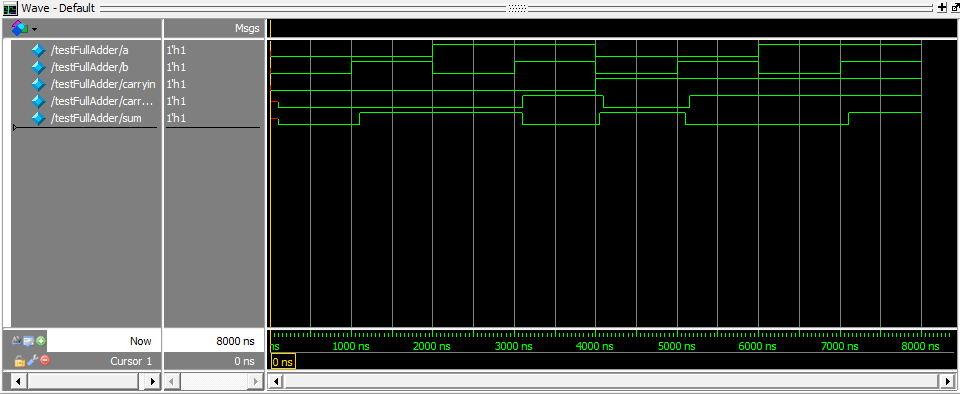
When the enable is LOW the outputs don’t change and when the enable is high the outputs start to change. The outputs react to each combinations of addr0 and addr1. At the combination of (addr0, addr1)=(0, 0) after 50ms of propagation delay out0 went up to high. Other combinations of addresses also made the output to change after the propagation delays.

1. Mux waveform



The waveforms match with the truth tables of mux. However there exists a propagation delay in the gates, so the output changes little bit later after the address changes. When we check the first output of (addr0, addr1) = (0, 0) it goes up after the delay and also after 2000ns when the addr1 changes from 0 to 1 the output show glitch because there is a mismatch of because there is additional inverter attached to addr0.

1. FullAdder waveform



The waveform matches with the truth table and because of the propagation delays in the gates. The carryout and the sum comes out after delays.